

# Device-Aware Diagnosis for Yield Learning in RRAMs

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**Abstract**—Resistive Random Access Memories (RRAMs) are now undergoing commercialization, with substantial investment from many semiconductor companies. However, due to the immature manufacturing process, RRAMs are prone to exhibit unique defects, which should be efficiently identified for high-volume production. Hence, obtaining diagnostic solutions for RRAMs is necessary to facilitate yield learning, and improve RRAM quality. Recently, the Device-Aware Test (DAT) approach has been proposed as an effective method to detect unique defects in RRAMs. However, the DAT focuses more on developing defect models to aid production testing but does not focus on the distinctive features of defects to diagnose different defects. This paper proposes a Device-Aware Diagnosis method; it is based on the DAT approach, which is extended for diagnosis. The method aims to efficiently distinguish unique defects and conventional defects based on their features. To achieve this, we first define distinctive features of each defect based on physical analysis and characterizations. Then, we develop efficient diagnosis algorithms to extract electrical features and fault signatures for them. The simulation results show the effectiveness of the developed method to reliably diagnose all targeted defects.

**Index Terms**—RRAM, defects, device-aware diagnosis, test

## I. INTRODUCTION

Resistive Random Access Memory (RRAM) is a viable technology for the next generation of non-volatile memories owing to its advantages, including high scalability, low access latency, and energy efficiency for AI computing [1, 2]. However, it is generally recognized that variations and defects in device characterization throughout the manufacturing process, create significant challenges [3–5]. Hence, there is a pressing need for a comprehensive understanding of manufacturing defects and the development of high-quality test solutions. Moreover, the seamless combination of testing with diagnosis is paramount in achieving a holistic approach to improving RRAM manufacturing processes and yield learning. Therefore, effective diagnosis methods are as important as defect detection to enable high volume detection [5, 6].

Although there are several works on test and diagnosis of RRAMs, most of the work focuses on detection rather than diagnosis. In 2009, Ginez *et al.* investigated coupling faults by simulating bridge defects as resistors [7]. In 2015, Chen *et al.* reported a dynamic write disturbance fault, and a March test to cover it [8]. In 2017, Li *et al.* leveraged judicious control of the sneak-paths to design a fault isolation technique and diagnosis algorithm [9]. In 2022, a March diagnosis algorithm was designed for distinguishing conventional RRAM defects

[5]. However, all these methods rely on *linear resistors* as the defect model, which is certainly insufficient to describe unique defects in the RRAM device itself because the device is inherently *non-linear* [10]. To address this challenge, the Device-Aware Test (DAT) approach was proposed [4, 11, 12]. The DAT approach considers the physical roots of defects and incorporates their impact into the technology parameters of the device, enabling accurate defect modeling and test generation for unique defects [4]. Although the DAT approach has demonstrated its power in modeling and testing RRAM-related unique defects, it is not practical to diagnose these defects, as its primary optimization focuses on *defect detection* instead of *defect diagnosis*. For instance, one test solution proposed in [10] for forming defects could detect other defects as well, thus it is inefficient for diagnosis. Therefore, a dedicated method of diagnosing unique defects is required to enhance the quality of RRAM fabrication further.

This paper focuses on the diagnosis of conventional and unique defects in RRAMs. We present a novel framework called Device-Aware Diagnosis (DA-Diagnosis), which goes one step further than DAT by utilizing the defect models obtained from DAT; the framework applies a systematical method to analyze physical manufacturing defects and extract their distinctive features for RRAM diagnosis. Thanks to the unique defect modeling of the DA method, unique and reliable fault signatures for each defect are obtained. DA-Diagnosis surpasses the limitation of existing memory diagnosis methodologies as it is a comprehensive approach that is based on defect origins and covers specific faults. The main contributions of this paper are:

- Present the framework of the DA-Diagnosis method for conventional and unique defects in RRAMs.
- Analyze and define distinctive features of all targeted RRAM defects, especially unique defects.
- Design diagnosis algorithms based on distinctive features.
- Demonstrate the effectiveness of developed diagnosis algorithms for targeted conventional and unique defects.

The rest of this paper is structured as follows. Section II establishes the RRAM basics. Section III presents the framework of the DA-diagnosis method for targeted defects. Section IV applies the proposed DA-diagnosis framework to the targeted defects. Section V validates designed diagnosis algorithms. Finally, Section VI discusses and concludes this paper.

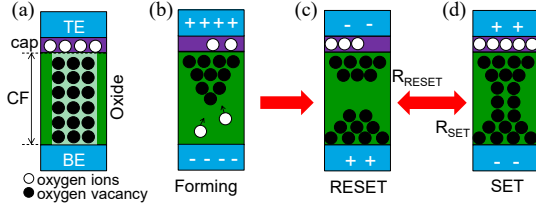


Fig. 1. Evolution of the conductive filament. (a) RRAM stack, (b) Forming, (c) RESET, (d) SET.

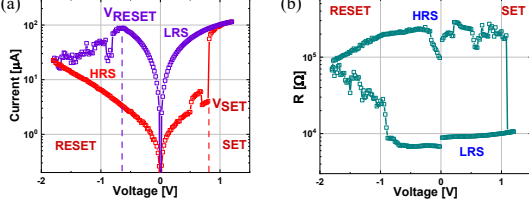


Fig. 2. RRAM electrical switching. (a) Switching I-V curve in log scale, (b) Switching R-V curve in log scale.

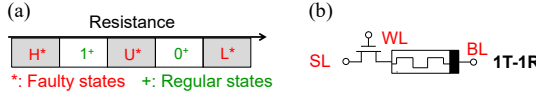


Fig. 3. RRAM technology. (a) RRAM resistance states, (b) 1T-1R cell.

## II. RRAM BASICS AND BACKGROUND

An RRAM device is a Metal-Insulator-Metal (MIM) stack, as shown schematically in Fig. 1 (a) [13]. In its organization, the middle metallic oxide is built with an extra capping layer in between the top and bottom metal electrodes (TE and BE). Typically, an RRAM device requires a forming process; it is a post-manufacturing step that involves applying a high voltage between two electrodes to form a *Conductive Filament* (CF) consisting of oxygen vacancies (OV), as shown in Fig. 1 (b).

The shape of the CF decides the different resistances of the RRAM. Fig. 2 shows the switching current-voltage (I-V) and resistance-voltage (R-V) curves. The generation of more OV (Fig. 1 (d)), which is referred to as a SET operation, causes the CF length to rise with a positive voltage from TE to BE ( $V_{TE}$ ) greater than the threshold ( $V_{TE} \geq V_{SET}$ ) [13]. Oppositely, the dissolution of the CF (see Fig. 1 (c)) is referred to as a RESET operation when  $V_{TE} \leq V_{RESET}$ . The resistance states after SET and RESET are referred to as  $R_{SET}$  and  $R_{RESET}$ .

The formation and dissolution of the CF is a result of the stochastic  $O^{2-}$  movement; this can cause cycle-to-cycle and device-to-device variations in the resistance [13]. Hence, the (binary) RRAM can be divided into 5 states, as shown in Fig. 3 (a) [4, 14, 15]: 1) the faulty extremely high conductance state ‘H’, 2) the correct low resistive state ‘1’, 3) the faulty undefined state ‘U’, 4) the correct high resistive state ‘0’, and 5) the faulty extremely low conductance state ‘L’.

Fig. 3 (b) shows a typical RRAM 1-Transistor-1-Resistor (1T-1R) cell with three terminals connecting with the Bit Line (BL), Source Line (SL), and Word Line (WL). The WL controls the transistor to make the data stored in the desired cells accessible. BLs and SLs are set to appropriate voltages for write (SET and RESET) and read operations.

Fig. 4 presents a  $3 \times 3$  1T-1R circuit architecture with related peripheral circuits [10]; it comprises the core memory cell

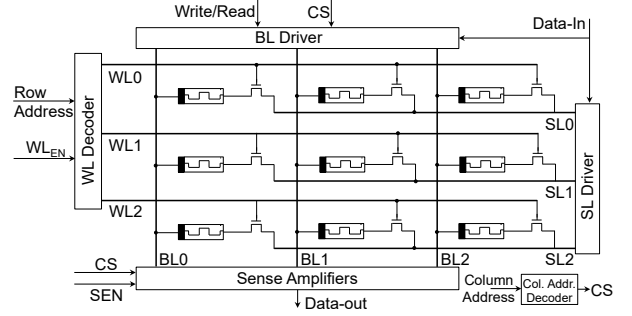


Fig. 4. Schematic of 1T-1R RRAM architecture [10].

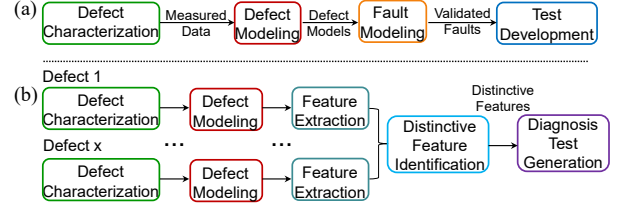


Fig. 5. Framework of RRAM test and diagnosis development: (a) DAT process, (b) DA-diagnosis process.

array and peripheral circuits. Cells in the same row share the same WL and SL, while those in the same column share the same BL. The peripheral circuit consists of the WL decoder, BL driver, and Sense Amplifier (SA) [16]. The decoder selects cells, the driver provides write and read currents, and the SA senses the current through the RRAM device to read cell states.

## III. METHODOLOGY FOR DEVICE-AWARE DIAGNOSIS

Fig. 5 (a) shows the DAT approach; it consists of four steps: defect characterization, defect modeling, fault modeling, and test development [4, 12]. DAT has been shown to be very powerful in modeling and testing unique defects in emerging memories such as RRAMs [17, 18] and STT-MRAMs [11]. It focuses on maximizing the fault/defect coverage while optimizing the test time. However, such an approach cannot be applied straightforwardly to diagnosis as it cannot uniquely identify which defect causes the detected fault. For example, the March test and DfT designed for Ion Depletion (ID) defects in RRAMs in [18] can detect other conventional defects; hence they fail to provide the distinctiveness for defects. Therefore, the DAT approach needs to be adapted for diagnosis.

Fig. 5 (b) shows the DA-diagnosis approach; it consists of five steps. Note that steps 1, 2, and 3 have to be repeated for each targeted defect (to be diagnosed); the results will be then processed to create a ‘feature dictionary’, which will be the basis to generate diagnosis test algorithms. Note also that steps 1 and 2 for DAT as well as for DA-diagnosis are the same. The platform was first applied for Spin-Transfer Torque Magnetic RAMs (STT-MRAMs) in [19], and adapted to apply for RRAMs in this work. In the rest of this section, we will discuss the five steps of the DA-diagnosis approach.

### A. Defect characterization

In this step, the targeted defects are determined. Defect models and characterization data of calibrated defects are used

to develop a library of defects and their features.

### B. Defect modeling

This step appropriately models defects. The conventional defects are modeled as linear resistors [20], while unique defects require DA defect modeling, which describes the impact of the defect on the device technology parameters and thereafter on electrical behavior and obtains a defective device model [4]. DA defect models have been shown to be accurate defect modeling of unique RRAM defects [4, 17, 18, 21].

### C. Feature extraction

This step extracts features of each defective device based on the way the defect manifests itself in the functional behavior of the memory. The features of RRAM refer to the electrical parameters of the memory device. For RRAM, these are  $V_{SET}$ ,  $V_{RESET}$ ,  $R_{SET}$ , and  $R_{RESET}$ ; they can be extracted from the simulation or measurement. Combining all extracted features for all targeted defects results in an initial feature dictionary.

### D. Distinctive feature identification

The distinctive features of each defect are selected from the feature dictionary. Here a distinctive feature indicates a unique behavior caused by one or more electrical parameters due to the presence of a defect; such behavior is uniquely associated with that defect. For example, a cell enters ‘H’ state only if a certain defect (i.e., over forming) is presented in the memory; no other defects can cause such behavior.

### E. Diagnosis test generation

Based on distinctive features, this step generates a set of diagnosis test algorithms being able to distinguish which defect is causing certain faults; i.e., if one or more tests from the set fails, then we can derive (based on the signature created) which defect does the memory suffer from. Note that in our analysis, we assume a single defect at a time. Other diagnosis methods based on Physical Failure Analysis (PFA) are not considered since it requires expensive, time-consuming, and destructive analysis [22]. Finally, the output of this step is the DA-Diagnosis algorithm for each defect.

## IV. APPLICATION OF THE METHODOLOGY FOR RRAMS

In this section, we follow the DA-Diagnosis framework to design diagnosis methods for targeted defects.

### A. Targeted defects and their characterizations

The targeted defects consist of conventional defects and unique RRAM defects.

1) *Conventional defects* [7, 20]: These consist of well-known interconnect and contact defects, which can cause opens, shorts, and bridges. They can be modeled accurately by *linear resistors* [7, 20], see Fig. 6 (a). Both write and read faults can be sensitized by these defects.

2) *Unique RRAM defects*: These consist of defects that are found inside the RRAM device due to fabrication imperfection. As of now, there are five unique defects known in the public domain; they are explained next.

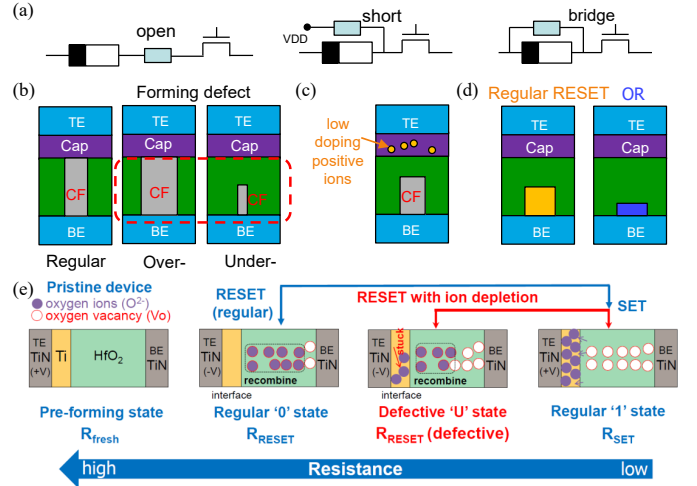


Fig. 6. Physical mechanism of defects. (a) Conventional defects [7, 20], (b) Forming defects [4], (c) IUSF [17], (d) OR [21], (e) ID [18].

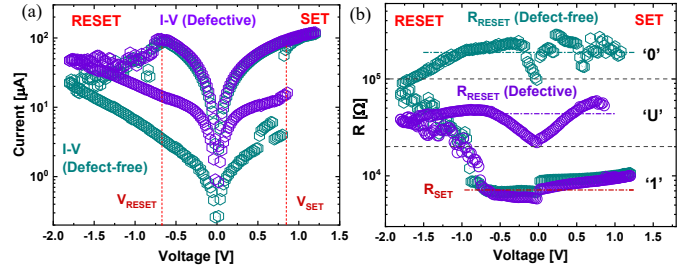


Fig. 7. Characterization of defect-free and ID-defective device: (a) I-V measurement, (b) R-V measurement.

a) *Over/under forming (O/UF)* [4, 23]: The forming defect is introduced by an inappropriate forming current. The external tester usually controls the forming current; hence an unstable voltage source may affect the forming process [15]. The forming defect may come in two variants: over (under) forming when a too-large (small) CF is generated, as presented in Fig. 6 (b), initializing to a resistance state that is much lower (higher) than the nominal LRS.

b) *Intermittent Undefined State Fault (IUSF)* [17]: As presented in Fig. 6 (c), the IUSF is related to imperfect capping layer doping or OF, which causes the RRAM device to *intermittently* change its switching mechanism from bipolar to complementary switching, leading to an undefined state during SET process.

c) *Ion Depletion (ID)* [18, 24]: As presented in Fig. 6 (e), the ID defect is caused by interface physical imperfections, which involve an increased oxygen trap of the defective capping layer, resulting in a lower recombination rate between insufficient  $O^{2-}$  and OV.

d) *Over RESET (OR)* [21]: As presented in Fig. 6 (d), the OR phenomenon is caused by a reduced  $O^{2-}$  storage capacity (oxygen affinity), and extra ions come back to recombine the CF, leading to an *intermittent* extremely high resistance state exceeding the HRS criteria.

For the characterizations, we perform I-V, R-V, and  $R_{SET}$ - $I_{forming}$  measurements for defects mentioned in Section III-A. For conventional defects, we characterize them with the RRAM compact model in [25] in Cadence's Spectre simu-

TABLE I  
FEATURE DICTIONARY OF TARGETED DEFECTS.

Defects		Electrical parameters							
		$R_{SET}$		$R_{RESET}$		$ V_{SET} $		$ V_{RESET} $	
Conventional	Interconnects & Contacts	$\uparrow, \downarrow, NA$	U L	$\uparrow, \downarrow, NA$	U L	$\uparrow, \downarrow, NA$		$\uparrow, \downarrow, NA$	
Unique	OF	$\downarrow$	H	NA		$\downarrow$		$\uparrow$	
	UF	$\uparrow$	U	$\uparrow$	L	NA		$\downarrow$	
	IUSF	$\uparrow$ (IB)	U	NA		NA		NA	
	ID	NA		$\downarrow$ (IB)	U	NA		NA	
	OR	NA		$\uparrow$ (IB)	L	$\uparrow$ (IB)		NA	

Note:  $\uparrow$ : increase;  $\downarrow$ : decrease; NA: not affected; (IB): intermittent behavior; H/U/L: faulty states

lation, following the process in [10, 26]. For unique defects, we have reused the characterization results produced in [4, 17, 18, 21, 23]. Measurements are produced on a  $7 \times 7$  1T-1R array. The I-V curves are performed by the Keysight B1500 parameter analyzer and extracted by Python. After that, the R-V can be converted from I-V measurements. For example, Fig. 7 (a) and (b) present measurements and compare those for defect-free and ID-defective devices. A current increase and  $R_{RESET}$  decrease can be observed for I-V and R-V curves of the defective device. Besides, we also investigate the relationship between resistance and forming currents ( $R_{SET}$ - $I_{forming}$ ) based on HfO<sub>2</sub>-RRAM measurements in [23]. Not all measurements are shown in this paper due to space limitations.

### B. Defect Modeling

In this step, we directly use linear resistance for conventional defects [20, 26] and DA-defect models of the 5 targeted unique defects reported in previous works in [4, 17, 18, 21].

### C. Feature Extraction

In this step, we summarize the feature dictionary for targeted defects through measurements and simulation in Table I. The symbols used in the table are listed as notations. For example, in the presence of IUSF, there is a certain probability that the  $R_{SET}$  increases intermittently. Especially, we present possible faulty states ('H', 'U', 'L') that are sensitized by each defect when  $R_{SET}$  and  $R_{RESET}$  are affected by defects as features.

### D. Distinctive feature identification

This step aims to identify distinctive features of each defect. If a feature is unique in each column of Table I, it is considered a distinctive feature. Consequently, distinctive features of targeted defects can be directly derived from Table I. For example, the *intermittently* (IB) increased  $R_{RESET}$  is identified as a distinctive feature for the OR defect; yet the permanent increased  $R_{RESET}$  is not a distinctive feature, since the same feature can also be found in the presence of conventional defects and UF. For the defects that have multiple distinctive features, we can select those that facilitate the most effective diagnosis. For the defects without distinctive features, we can also consider combining features to make them distinctive. Next, we present distinctive features of each targeted defect.

1) *Conventional defects*: The impact on features of conventional defects also depends on the precise type (bridges, shorts, or opens), range, and location of the defect. For example, we observed that bridges in parallel with the cell affect both  $R_{SET}$  and  $R_{RESET}$ ; while some shorts affect only one of the resistive states [10, 26]. Hence, conventional defects lack distinctive features, which will be discussed later.

2) *OF*: As presented in Table I, the 'H' state of  $R_{SET}$  can be considered as the distinctive feature because other defects cannot make the cell switch to 'H'. Besides,  $|V_{RESET}|$  is another distinctive feature compared with other *unique defects*. We can even weaken the RESET write pulse to better identify the unique  $|V_{RESET}|$ .

3) *UF*: As presented in Table I, there is no ensured distinctive feature of UF. However,  $|V_{RESET}|$ ,  $R_{SET}$ , and  $R_{RESET}$  are distinctive features compared with other unique defects. Especially, the 'L' state  $R_{RESET}$  can be combined with other features to facilitate diagnosis, which will be discussed later.

4) *IUSF*: As presented in Table I,  $R_{SET}$  is the distinctive feature of IUSF. Especially, this defect occurs intermittently with different cycles owing to the intrinsic stochasticity. The intermittent behavior indicates that the defect has a probability of occurring rather than exhibiting a constant resistance in different cycles, like the conventional defects.

5) *ID*: As presented in Table I, an intermittently reduced  $R_{RESET}$  is the distinctive feature. Other defects, such as conventional defects, can also lead to reduced  $R_{RESET}$  but without the intermittent behavior.

6) *OR*: As presented in Table I, intermittently increased  $|V_{SET}|$  and  $R_{RESET}$  are distinctive features of OR.

In conclusion, among those unique defects, OF sensitizes unique 'H' state faults; IUSF, ID, and OR all exhibit intermittent faulty behavior owing to the intrinsic stochasticity [13]. These specific faulty behaviors are impossible to occur in the presence of conventional defects. Hence, these unique defects will not be mixed with conventional defects. Unfortunately, UF may sensitize faults that are also sensitized by conventional defects; hence, it is critical to distinguish them.

To achieve this, we propose a process based on the comparison of faults that are sensitized by different defects. The assumption is that every defect sensitizes a different set of faults. Hence, comparing these fault sets of each defect can facilitate the diagnosis. The whole process is: 1) obtain a set of sensitized faults in the presence of all defects, 2) compare obtained fault sets of the targeted unique defects with the other fault sets; diagnose the defect as either a conventional or an unknown defect when there is no overlap in the comparison. If there is an overlap, proceed to the third step for further diagnosis, and 3) further compare fault sets of unique defects with the set of faults that are sensitized by all conventional defects. If there is no overlap in this comparison, diagnose the defect as either a conventional or a unique defect. Otherwise, a diagnosis cannot be guaranteed. Another benefit of this process is that once we complete the first step, we will be able to identify the location of faulty cells, allowing us to save time by applying the algorithm only to the faulty cells. In our case study, all faults sensitized by UF do not overlap with conventional defects of any strength [10, 26]; hence, it is possible to distinguish them.

### E. Diagnosis Test Generation

This step generates DA-Diagnosis methods for all RRAM-targeted defects. The diagnosis design first aims to distinguish

TABLE II  
OVERVIEW OF DIAGNOSIS FOR UNIQUE DEFECTS.

Defect	Mechanism	Related steps in RRAM fabrication	Test method	Diagnosis algorithm	Notation
OF	Higher forming current	Forming step	$\Downarrow (w0, w1, w0)$ ;	$\Downarrow (w1, r1)$	Requires multiple references
UF	Lower forming current	Forming step	$\Downarrow (r0)$ ; $\Downarrow (w1, r1)$ [10]	$\Downarrow (w0, r0, w1, r1)$	
IUSF	Reduced oxygen storage capability	(1) Over forming (2) Capping layer doping, Annealing	$\Downarrow (w0, w1, r1)^i$ [17]	$\Downarrow (w0, w1, r1)^i$	Requires multiple references Requires algorithm repetitions
ID	$O^{2-}$ depletion, interface imperfection	HfO <sub>2</sub> or TiO <sub>2</sub> deposition, Annealing	$\Downarrow (w1)$ ; $\Downarrow (w0, r0)$ [18]	1. $\Downarrow (w1)$ ; $\Downarrow (w0, r0)$ ; $\Downarrow (w1, r1)$ 2. $\Downarrow (w1, w0, r0)^j$	
OR	Reduced oxygen storage capability	TiO <sub>2</sub> deposition, Annealing	$\Downarrow (w1)$ ; $\Downarrow (w0, r0)$ [21]	1. $\Downarrow (w1, r1)$ ; $\Downarrow (w0, r0)$ 2. $\Downarrow (w1, w0, r0)^k$	

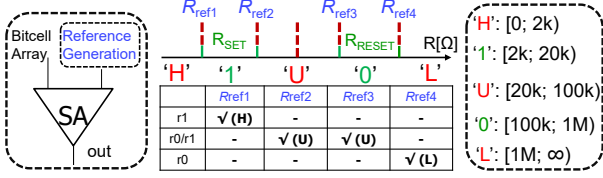


Fig. 8. Reference settings and resistance state specifications.

between conventional and unique defects and then applies patterns to further distinguish which unique defect is present.

From the distinctive features obtained in Table I, it is necessary to detect not only regular '0' and '1' states, but also faulty 'H', 'U', and 'L' states. In this paper, the diagnosis methods are based on March algorithms with adjustable read operations. A regular SA design [16] with multiple yield learning references is applied. Fig. 8 shows the implementation of the reference setting for three specific read operations. Those references are set according to the defined resistance states and with a checkmark to indicate the reference used. For example, the reference ( $R_{ref1}$ ) equal to the minimum  $R_{SET}$  is applied to detect the 'H' state. Two references ( $R_{ref2}$ ,  $R_{ref3}$ ) are applied to detect 'U' from '0' and '1'. The reference ( $R_{ref4}$ ) equal to the maximum  $R_{RESET}$  is applied to detect the 'L' state. Next, we apply the above process and present the diagnosis designs for each defect. Table II summarizes the final result of this section.

1) *Conventional defects*: We follow the above process (compare sensitized faults) to distinguish conventional defects from unique defects, further diagnosis for types and locations of conventional defects is out of the scope of this paper.

2) *OF*:  $R_{SET}$  serves as a distinctive feature of OF. Hence, we design the diagnosis method by reading the 'H' state (with equivalent  $R_H$  shown in Fig. 9) of the faulty cell to identify fault origins in the presence of OF as follows:  $\{\Downarrow (w1, r1)\}$ . Here,  $\Downarrow$  indicates that operations are performed with irrelevant addressing direction;  $w1$  denotes write 1 and  $r1$  read 1 (using  $R_{ref1}$ ). In case of the OF defect,  $r1$  returns 'H'.

3) *UF*: UF may cause the defective cell into an 'L' state (see Fig. 9). Therefore, we design the March algorithm:  $\{\Downarrow (w0, r0, w1, r1)\}$ . Here, the  $r0$  operation is performed by applying  $R_{ref4}$ . If returned values are (L, 0), the cell has a UF defect. If there are (L, 1), the cell may have an OR defect.

4) *IUSF*: The intermittent  $R_{SET}$  is the distinctive feature of IUSF. The affected  $R_{SET}$  exhibits an intermittent 'U' state during the SET process with a low probability (up to 1.068%) [17]. To distinguish IUSF from other defects, it is sufficient to detect  $R_{SET}$  with the following repeated

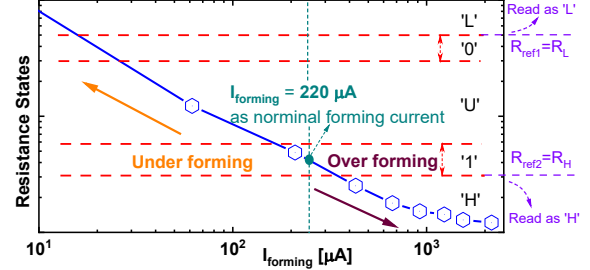


Fig. 9. Diagnosis for forming defects.

algorithm:  $\{\Downarrow (w0, w1, r1)^i\}$  (i.e., repeating  $w0$ ,  $w1$  and  $r1$  operations for ' $i$ ' times). The  $r1$  here applies  $R_{ref2}$  and  $R_{ref3}$  to detect the 'U' state. The probability of IUSF occurrence  $P_{IUSF}$  can result in the diagnostic probability:  $P_d = 1 - (1 - P_{IUSF})^i$ . From the measurement,  $i = 644$  can achieve a 99% Fault Coverage (FC). If the values obtained from the algorithm are oscillating (U), the defective cell suffers from an IUSF.

5) *ID*: The ID-defective device is stuck at the intermediate state 'U' (45% cycles). For diagnosis, we design the algorithm:  $\{\Downarrow (w1); \Downarrow (w0, r0); \Downarrow (w1, r1)\}$ . This algorithm consists of three elements: 1) apply  $w1$  for initialization, 2) apply  $1w0$  and  $r0$  using  $R_{ref2}$ ,  $R_{ref3}$  to detect 'U', and 3) apply  $\Downarrow (w1, r1)$  to check whether the  $R_{SET}$  is in nominal '1' state (using  $R_{ref1}$ ). Note that the third element is necessary to distinguish ID from OF (i.e., OF may switch cell into 'H'). If read values return (U, 1), the ID defect is diagnosed (assume it occurs at this cycle). To target intermittent behavior, another algorithm:  $\{\Downarrow (w1, w0, r0)^j\}$  can be applied ( $r0$  applies  $R_{ref2}$ ,  $R_{ref3}$  to detect 'U'). The second algorithm is expensive but guaranteed for ID diagnosis (an FC=99% requires  $j=8$ ).

6) *OR*: The proposed diagnosis algorithm is:  $\{\Downarrow (w1, r1); \Downarrow (w0, r0)\}$ . The first element is to initialize the cell to the '1' state and read the state. The second element is applied to identify whether the cell switched to 'L' owing to the OR. The  $r0$  here applies  $R_{ref4}$  to detect the 'L' state. If the read values are (1, L), the OR is diagnosed (assume OR occurs at this time). Again, we design another algorithm:  $\{\Downarrow (w1, w0, r0)^k\}$  to guarantee the high probability of diagnosis for OR (an FC=99% requires  $k=11$ ).

## V. VALIDATION OF DIAGNOSIS ALGORITHMS

Finally, we validate the diagnosis algorithms in Table II through simulation, following the process in Fig. 10. For each targeted defect injected in the circuit netlist, the designed diagnosis algorithms are applied. After that, the outputs of algorithms are extracted and compared with expected outputs



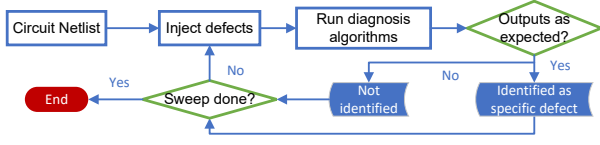


Fig. 10. Flow chart of diagnosis algorithm verification.

TABLE III  
VALIDATION WITH OF-DEFECTIVE CELL.

Defect	Expected output	Actual output	Diagnosed?
OF	H	H	Yes
UF	L, 0	1, 1	No
IUSF	U	1	No
ID	U, 1	1, H	No
OR	1, L	1, 1	No

to validate whether the algorithm can identify the defect. Once all algorithms are simulated, the next defect will be injected and the process will be repeated. Note that we focus more on applying algorithms designed for unique defects; the identification of conventional defects can be achieved by comparing different sets of faults that are sensitized by different defects.

Table III shows the validation result for the OF defect as an example. In the simulation setup, we follow the above process. All designed diagnosis algorithms are applied in the presence of OF defect. Table III shows expected and actual outputs for each applied algorithm. Only if the actual read output is the same as expected, the corresponding defect is diagnosed. For example, both the actual and expected outputs of the algorithm designed for OF are H, which means the defect is identified as OF. However, the actual outputs (1, 1) of the algorithm designed for OR are different from its expected outputs (1, L), which indicates the defect is not OR.

## VI. DISCUSSION AND CONCLUSION

This paper introduced the DA-diagnosis framework to detect conventional and unique defects in RRAMs. First, it identifies distinctive features for every defect based on physical analysis and characterization. Next, efficient mechanisms are developed that detect these distinctive features and thus efficiently diagnose the defects. We can conclude the following:

- **Effectiveness:** The results demonstrate that all RRAM defects can be uniquely identified with the DA-Diagnosis framework. This is because distinctive features for every defect are identified, which allows for tailored diagnosis solutions to only detect them. As such, the resulting diagnosis solutions are accurate and fast.
- **Applicability:** The framework can be applied to currently unknown RRAM defects and other memory technologies as well. Once new RRAM defects are identified, they need to be modeled using the DAT approach. Based on the resulting models and the measurements of the defect, distinctive features of this defect can be identified as well. Next, a diagnosis solution can be developed that uniquely identifies this defect. A similar argumentation holds for other memory technologies: first, defects need to be modeled, then distinctive features can be identified, and finally, effective diagnosis solutions can be developed.

- **Defect Modeling:** The usage of accurate defect models gives this framework its strength, but their development is limited. From earlier work on DAT, it can be concluded that defect identification and accurate defect modeling are not straightforward tasks [17]. This is because the defect needs to be deeply characterized with large amounts of measurement data, and the physics of its behavior properly modeled. Only once the appropriate defect model is developed, the distinctive features can be reliably identified and an effective diagnosis solution developed.

## REFERENCES

- [1] H.-S. P. Wong *et al.*, “Metal–Oxide RRAM,” *P. IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012.
- [2] S. Hamdioui *et al.*, “Applications of Computation-In-Memory Architectures based on Memristive Devices,” in *DATE*, 2019, pp. 486–491.
- [3] D. Niu *et al.*, “Impact of Process Variations on Emerging Memristor,” in *DAC*, 2010, pp. 877–882.
- [4] M. Fieback *et al.*, “Device-Aware Test: A New Test Approach Towards DPPB Level,” in *ITC*, 2019, pp. 1–10.
- [5] S.-C. Hung *et al.*, “Fault Diagnosis for Resistive Random-Access Memory and Monolithic Inter-tier Vias in Monolithic 3D Integration,” in *ITC*, 2022, pp. 118–127.
- [6] R. Adapa *et al.*, “Accelerating Diagnosis via Dominance Relations between Sets of Faults,” in *VTS*, 2007, pp. 219–224.
- [7] O. Ginez *et al.*, “Design and Test Challenges in Resistive Switching RAM (ReRAM): An Electrical Model for Defect Injections,” in *ETS*, 2009, pp. 61–66.
- [8] Y.-X. Chen *et al.*, “Fault Modeling and Testing of 1T1R Memristor Memories,” in *VTS*, 2015, pp. 1–6.
- [9] T. Li *et al.*, “Sneak-Path Based Test and Diagnosis for 1R RRAM Crossbar Using Voltage Bias Technique,” in *DAC*, 2017, pp. 1–6.
- [10] M. Fieback *et al.*, “Defects, Fault Modeling, and Test Development Framework for RRAMs,” *JETC*, vol. 18, no. 3, pp. 1–26, 2022.
- [11] L. Wu *et al.*, “Electrical Modeling of STT-MRAM Defects,” in *ITC*, 2018, pp. 1–10.
- [12] S. Hamdioui *et al.*, “Device Aware Test for Memory Units,” *Patent No. NL 2023751*, 2021.
- [13] S. Yu *et al.*, “On the Stochastic Nature of Resistive Switching in Metal Oxide RRAM: Physical Modeling, Monte Carlo Simulation, and Experimental Characterization,” in *IEDM*, 2011, pp. 17–3.
- [14] N. Z. Haron *et al.*, “DFT Schemes for Resistive Open Defects in RRAMs,” in *DATE*, 2012, pp. 799–804.
- [15] C. Y. Chen *et al.*, “RRAM Defect Modeling and Failure Analysis Based on March Test and a Novel Squeeze-Search Scheme,” *TC*, vol. 64, no. 1, pp. 180–190, 2015.
- [16] W. Zhao *et al.*, “Synchronous Non-Volatile Logic Gate Design Based on Resistive Switching Memories,” *T CIRCUITS-I*, vol. 61, no. 2, pp. 443–454, 2014.
- [17] M. Fieback *et al.*, “Intermittent Undefined State Fault in RRAMs,” in *ETS*, 2021, pp. 1–6.
- [18] H. Xun *et al.*, “Device-Aware Test for Ion Depletion Defects in RRAMs,” in *ITC*, 2023, pp. 246–255.
- [19] A. Aouichi *et al.*, “Device Aware Diagnosis for Unique Defects in STT-MRAMs,” in *ATS*, 2023, pp. 1–6.
- [20] S. Hamdioui *et al.*, “An Experimental Analysis of Spot Defects in SRAMs: Realistic Fault Models and Tests,” in *ATS*, 2000, pp. 131–138.
- [21] H. Xun *et al.*, “Characterization and Test of Intermittent Over RESET in RRAMs,” in *ATS*, 2023, pp. 1–6.
- [22] S.-Y. Liu *et al.*, “SiGe Profile Inspection by Using Dual Beam FIB System in Physical Failure Analysis,” in *IPFA*, 2013, pp. 490–492.
- [23] A. Grossi *et al.*, “Fundamental Variability Limits of Filament-Based RRAM,” in *IEDM*, 2016, pp. 4.7.1–4.7.4.
- [24] B. Chen *et al.*, “Physical Mechanisms of Endurance Degradation in TMO-RRAM,” in *IEDM*, 2011, pp. 12.3.1–12.3.4.
- [25] H. Li *et al.*, “A SPICE Model of Resistive Random Access Memory for Large-Scale Memory Array Simulation,” *EDL*, vol. 35, no. 2, pp. 211–213, 2014.
- [26] H. Xun *et al.*, “Data Background-Based Test Development for All Interconnect and Contact Defects in RRAMs,” in *ETS*, 2023, pp. 1–6.